FRINGING CAPACITOR STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of United States Patent Application No. 09/765,200 filed on January 18, 2001, which claims the benefit of U.S. Provisional Application No. 60/229533, filed on September 5, 2000, both of which are incorporated by referenced in their entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates generally to capacitors, and in particular to capacitors that are implemented within a semiconductor device.

Discussion of the Related Art

[0003] Conventional capacitors that are fabricated on semiconductor devices for storing charge are typically configured as metal-to-metal capacitors (MOMs). Referring to Figure 1, the construction of a typical MOM 10 is illustrated. The MOM 10 includes two electrodes 12 that are formed on conductor layers 14 and 16 that are separated by a dielectric 18. A substrate 19 forms a base for the MOM 10. In addition to the device capacitance which is formed between the electrodes, there is also an undesirable parasitic capacitance that is formed between the substrate 19 and adjacent electrode. In many conventional devices, the parasitic capacitance may exceed 20% of the value of the capacitance between the electrodes of the capacitor. To increase the value of capacitance, generally either the plate area of the MOM

is increased, or the dielectric thickness is decreased. Both of these options have drawbacks. Increasing the plate area causes a further undesirable increase in the parasitic capacitance, while reducing the dielectric thickness requires an extra process step that significantly increases the cost of the device. In addition, the matching characteristics of conventional semiconductor capacitors are deficient due to the non-symmetrical effect of external fields on adjacent capacitors.

SUMMARY OF THE INVENTION

[0004] The present invention provides a circuit and method for a fringing capacitor. The fringing capacitor includes at least two conductor layers spaced apart from each other. Each conductor layer includes at least two portions. The portions include odd ones alternating with even ones. Adjacent odd ones and even ones of the portions are spaced apart. The odd ones of the portions on a first one of the conductor layers are configured to substantially overlay the odd ones of the portions on an adjacent one of the conductor layers. The even ones of the portions on the first one of the conductor layers are configured to substantially overlay the even ones of the portions on the adjacent one of the conductor layers. The odd ones of the portions on the first one of the conductor layers are electrically coupled together and to the even ones of the portions on the adjacent one of the conductor layers, thereby defining a first electrode. The even ones of the portions on the first one of the conductor layers are electrically coupled together and to the odd ones of the portions on the adjacent one of the

conductor layers, thereby defining a second electrode. A dielectric is interposed between the first and second electrodes.

[0005] For a more complete understanding of the invention, its objects and advantages, reference may be had to the following specification and to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 illustrates a conventional metal-on-metal capacitor;

[0007] Figure 2A illustrates a side-view of an embodiment of a fringing capacitor in accordance with the principles of the invention;

[0008] Figure 2B illustrates a top-view of an embodiment of a fringing capacitor in accordance with the principles of the invention;

[0009] Figure 3A illustrates a side-view of a presently preferred embodiment of a fringing capacitor in accordance with the principles of the invention;

[0010] Figure 3B illustrates a top-view of a presently preferred embodiment of a fringing capacitor in accordance with the principles of the invention;

[0011] Figures 4A, 4B, and 4C illustrate side and top-views of split-capacitance embodiments of a fringing capacitor in accordance with the principles of the invention; and

[0012] Figure 5 is a schematic diagram that represents a split-capacitance embodiment of a fringing capacitor in accordance with the principles of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0013] Referring to Figures 2A and 2B, illustrated are side and top views of a presently preferred embodiment of a fringing capacitor 20 fabricated on a semiconductor substrate 22 in accordance with the principles of the present invention. The fringing capacitor is particularly suitable for fabricating the device by using a conventional thin metal oxide process. The thin metal oxide process advantageously is less costly than complementary metal oxide semiconductor (CMOS) processes. However, using other semiconductor processes such as CMOS are also within the scope of the invention. The fringing capacitor 20 is particularly suitable for applications that require matched capacitors and high-density packaging.

[0014] The fringing capacitor 20 has a positive electrode 21 and a negative electrode 23. The positive and negative electrodes 21 and 23 are configured so that the device capacitance is formed between a combination of intralayer conductors as well as interlayer conductors. The fringing capacitor 20 includes two or more conductor layers 24 separated by associated dielectric layers 26 for forming interlayer capacitance. Dielectric layers 26 and conductor layers 24 are alternately stacked upon the substrate 22. A first dielectric layer 26a is deposited on the substrate 22. Then a first conductor layer 24a is fabricated on top of the first dielectric layer 26a. The dielectric layers 26 and conductor layers 24 continue to be alternately deposited to whatever number of layers is selected.

[0015] The conductor layers are preferably formed from aluminum, however any suitable conductive material is within the scope of the invention including copper, polysilicon, tungsten, gold, and silicon alloys such as

titanium silicide. Fabricated on each of the conductor layers 24 are multiple conductor legs 28 for forming an intralayer capacitance, Cf. The conductor legs 28 are formed to follow substantially parallel paths with a dielectric disposed between them. Adjacent conductor legs 28 are coupled to opposing electrodes. Preferably, the conductor legs 28 are configured to follow straight runs with every other conductor leg being coupled to a common electrode polarity. However, it is within the scope of the invention for the conductor legs 28 to have other path configurations such as circular, L-shaped, and spiral. Adjacent conductor legs are preferably separated approximately by a distance d_h along the path of the conductors so that an intralayer capacitance, Cf, is formed between the adjacent conductor legs. In the presently preferred embodiment, the distance d_h is selected to be 0.3 um.

[0016] Similarly, the conductor legs 28 on each layer are arranged to overlay the conductor legs 28 on adjacent conductor layers so that an interlayer capacitance, Ca, is formed between the conductor legs 28 of the adjacent conductor layers. Preferably, the dielectric layer 24 that is sandwiched between the adjacent conductor layers 28 is fabricated with a uniform thickness of d_v. In the presently preferred embodiment the dielectric layers 24 are fabricated with a thickness d_v of 1 um. The total capacitance, Cf, of the device is equal to the combination of Ca plus Cf. Preferably, Ca comprises about 20% of the total capacitance and Cf comprises about 80% of the total capacitance.

[0017] A parasitic capacitance, C_b, is also formed, being caused by the interaction between the substrate 22 and the nearest conductor layer 24. The ratio Cb/Ct provides a figure of merit indicating the quality of the fringing

capacitor 20. The lower the value of Cb/Ct, the higher the quality of the fringing capacitor 20. The value of Cb/Ct can be driven lower by increasing the number of conductor legs 28 on each conductor layer 24, and by increasing the number of conductor layers 24.

[0018] The fringing capacitor 20 is preferably fabricated with a total of three conductor layers. However, using two or more conductor layers 24 is within the scope of the invention. In conventional semiconductor capacitors, the value of the parasitic capacitance coupled to the substrate typically exceeds 20% of the value of the capacitance formed between the conductor layers. Relying on the fringing capacitance as well as employing multiple conductor layers 24 in the present invention improves the volumetric efficiency and reduces the value of parasitic capacitance, Cb, to less than 20% of the total capacitance.

[0019] Referring to Figures 3A and 3B, a second embodiment of a fringing capacitor 40 in accordance with the principles of the invention is illustrated. The fringing capacitor 40 is similar to fringing capacitor 20 in function with corresponding elements numbered in the range 40-49, except that fringing capacitor 40 includes a guardband 50 for attenuating coupling between the fringing capacitor 40 and external electromagnetic fields. The guardband 50 is preferably formed from a conductive material such as polysilicon, aluminum, and copper. In the preferred embodiment, the guardband 50 is provided on each conducting layer 44 and substantially encircles the electrodes of fringing capacitor 40. However, the scope of the invention includes providing the guardband on less than all of the conducting layers 44, and only running the guardband 50 along one side of the fringing

capacitor 40. In addition, the guardband 50 may be included on layers either above or below the fringing capacitor. Preferably, the guardband 50 is spaced from the conductors a distance dg that is approximately twice the distance dh between adjacent conductor legs 48. The distance dg is selected to minimize the parasitic fringing capacitance that is formed between the guardband 50 and the conductor legs 48, while at the same time maintaining a volumetrically efficient fringing capacitor 40. To maintain a predetermined ratio between the capacitance of the fringing capacitor 40 and the parasitic capacitance formed from the guardband 50, the distance dg is preferably increased when there are fewer conductor layers 44 or conductor legs 48, and the distance dg is preferably decreased when there are more conductor layers 44 or conductor legs 48. Preferably the line width of the guardband 50 is selected to be the same as the conductor legs 48, however the scope of the invention is not limited by the line width that is selected. Preferably the guardband 50 is coupled through a low impedance to a voltage potential such as ground reference, however the scope of the invention includes permitting the guardband to float with respect to system voltage potentials.

[0020] Referring to Figure 4A, an embodiment of a split-capacitance fringing capacitor 70 in accordance with the principles of the invention is shown. The split fringing capacitor 70 is particularly suitable in matched capacitor applications such as sample and hold capacitors, capacitor arrays in D/A and A/D converters, and especially multiplying D/A converters. The split-capacitance fringing capacitor 70 includes a first fringing capacitor 80 and a second fringing capacitor 100. The first fringing capacitor 80 is similar to fringing capacitor 20 in structure with corresponding elements numbered in

the range 80-89, except that fringing capacitor 80 divides the conductor legs 88 to form two capacitors C1 and C2'. The second fringing capacitor 100 is also similar to fringing capacitor 20 in structure with corresponding elements numbered in the range 100-109, except that fringing capacitor 100 likewise divides the conductor legs 108 to form two capacitors C2 and C1'. Capacitors C1 and C1' are interconnected forming a first capacitor, and capacitors C2 and C2' are interconnected forming a second capacitor. Preferably, C1, C1', C2, and C2' have equivalent capacitances, however the scope of the invention includes forming the capacitors with dissimilar capacitances as well as asymmetrical capacitances such as C1=C2 and C1'=C2', or C1=C2=C1'=C2'.

[0021] Referring to Figure 4B, another embodiment of a split-capacitance fringing capacitor 70' in accordance with the principles of the invention is shown. The split fringing capacitor 70' is similar to split fringing capacitor 70, except that split fringing capacitor 70' includes guardbands 72 and 74 to shield the components of the split fringing capacitor 70'.

[0022] Referring to Figure 4C, a top-view of an embodiment of a split-capacitance fringing capacitor 110 in accordance with the principles of the invention is shown. The split-capacitance fringing capacitor 110 includes four fringing capacitors 116-119, preferably arranged side-by-side forming a two-by-two square. The fringing capacitors 116-119 are similar in function and construction to fringing capacitors described in earlier sections of this specification. Preferably, one capacitor of a set of matched capacitors is formed by cross-connecting the fringing capacitors 116 and 119. A second capacitor of a set of matched capacitors is formed by cross-connecting the

fringing capacitors 117 and 118. Cross-connecting the fringing capacitors minimizes the impact of coupling between the fringing capacitors 116-119 and external electromagnetic fields.

[0023] Additionally referring to Figure 5, capacitors C1 and C1' are interconnected forming capacitor Ca, and capacitors C2 and C2' are interconnected forming capacitor Cb. Preferably, C1, C1', C2, and C2' have equivalent capacitances, however the scope of the invention includes forming the capacitors with dissimilar capacitances as well as asymmetrical capacitances such as C1=C2 and C1'=C2', or Ca≠Cb and C1≠C2≠C1'≠C2'. Preferably, a guardband 72 in accordance with the above description related to fringing capacitor 40, is interposed between the first and second fringing capacitors 80 and 100 to attenuate coupling between the two fringing capacitors 80 and 100. In addition, outer guardbands 74 in accordance with the above description, preferably encircle the split-capacitance fringing capacitor 70'. Preferably, the fringing capacitors 80 and 100 include an even number of ten or more conductor legs 88 and 108 on three or more conductor layers 84 to facilitate splitting the capacitors into even valued devices, providing a matching property for the split-capacitance fringing capacitor 70' of about 0.1%. Increasing the number of conductor legs 88 and 108, and maintaining an even number of conductor legs 88 and 108 improves the matching property of the split-capacitance fringing capacitor 70'.

[0024] Thus it will be appreciated from the above that as a result of the present invention, a circuit and method for constructing a capacitor is provided by which the principal objectives, among others, are completely fulfilled. It will be equally apparent and is contemplated that modification

and/or changes may be made in the illustrated embodiment without departure from the invention. Accordingly, it is expressly intended that the foregoing description and accompanying drawings are illustrative of preferred embodiments only, not limiting, and that the true spirit and scope of the present invention will be determined by reference to the appended claims and their legal equivalent.